REMARKS

Present Status of the Application

This is a full and timely response to the outstanding non-final Office Action mailed on July 21, 2003. Claims 1-19 remain pending of which claims 1, 6, 12, 15 and 16 have been amended to more explicitly and more clearly describe the claimed invention. It is believed that no new matter is added by way of these amendments made to the claims or specification or otherwise to the application.

The Applicants have most respectfully considered the remarks set forth in this Office Action. Regarding the obviousness rejections, it is however strongly believed that the cited references are deficient to adequately teach the claimed features as recited in the amended claims. The reasons that motivate the above position of the Applicants are discussed in detail hereafter, upon which reconsideration of the claims is most earnestly solicited.

Response to 35 U.S.C. 103 rejection

Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al. (US ,200,875 B1, Jang hereinafter) in view of Jeong (US 5,960,310).

Claims 1, 6, 12, 15 stand rejected under 35 U.S.C. 103(a) as purportedly being unpatentable over the US patent '875 to Jang in view of US patent '310 to Jeong. As described in detail hereinafter, Applicant respectfully asserts that Jang in view of Jeong is legally deficient

for the purpose of rendering claim 1 or 8 unpatentable for at least the reason that not every element of the claims was taught or suggested by cited reference such that the invention as a whole would have been obvious to one of ordinary skill in the art. In particular, Applicants respectfully assert that neither Jang nor Jeong teaches or discloses "*...an etching selectivity between the dielectric layer and the dielectric liner layer is high...and ...using the dielectric liner layer as an etch stop...*" as substantially taught in claims 1, 6 and 12, and "*...the dielectric liner layer is converted into second sidewall spacers for the first gate and the second gate...*" as substantially taught in claims 1 and 15. The present invention teaches a method for forming a self-aligned contact window between gates, wherein a thin liner layer is first formed over the gates structures, followed by forming a dielectric layer on the liner layer, wherein the etching selectivity between the dielectric layer and the liner layer is high. Further, using the liner layer as an etch stop and without planarizing the dielectric layer, the dielectric layer is patterned, followed by patterning the liner layer to form a contact window between the neighboring gates. Consequently, a sufficient protection is provided to the gates during the self-aligned contact window process.

Jang teaches forming a silicon oxide layer 30 over the semiconductor device and patterning it without planarizing it to form a self-aligned contact window. However, as recognized by the Office Action, Jang fails to teach forming a liner layer having a different etching selectivity from the silicon oxide layer. The formation of the liner layer, which serves as an etch stop, as taught in the present invention is to provide protection to the gates during the contact window process. Moreover, the liner layer is subsequently converted into a second

spacer for the gate structures in the present invention. Therefore in the absence of a liner layer, Jang fails to even imply forming a second spacer.

Contrary to the Office assertion, Applicants submit that Jeong does not teach forming a liner layer or a liner layer having an etching selectivity different from the subsequently formed dielectric layer so as to serve as an etch stop layer. Instead, Jeong teaches forming the first insulating layer 77 and the third insulating layer 81 with the similar type of material (col. 6, ln 36-65), so that they are etched in a single photolithographic step to form the contact holes thereby exposing the patterned wiring layers (col. 6, ln 66 to col. 7, ln. 3). There is no where in Jeong that either explicitly teaches or implicitly suggests a liner layer having an etching selectivity different from the overlying dielectric layer since in Jeong, the patterned wiring layer 75a serves as an etch stop. Further, the present invention teaches converting the liner layer to second spacers for the gates. Meanwhile, in the absence of a liner layer, neither Jeong nor Jang teaches converting the liner layer into second spacers.

For at least these reasons, Applicants respectfully assert that claims 1, 6, 12, 15 patentably define over Jeong in view of Jang. Since claims 2-5, 7-11, 13-14, 16-19 are dependent claims which further define the invention recited in claims 1, 6, 12, 15, respectively, Applicants respectfully assert that these claims also are in condition for allowance. Thus, reconsideration and withdrawal of this rejection are respectively requested.

Application N .: 09/920,390 **Docket No.: JCLA4757-CIP-R**

CONCLUSION

For at least the foregoing reasons, it is believed that the presently pending claims 1-19are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : 11/3/2003

Jiawei Huang
Registration No.: 43,330

J.C. Patents
4 Venture, suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax : (949) 660-0809